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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. ITL.0499US

In Re Application Of: **Christopher J. Kemp; Christop P. Menzel**

Serial No.	Filing Date	Examiner	Group Art Unit
09/751,993	December 29, 2000	Roberto Jose Rios Cuevas	2836

Invention: **Converting Sensed Signals**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **November 26, 2003**

The fee for filing this Appeal Brief is: **$330.00**

☒ A check in the amount of the fee is enclosed.

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☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **January 20, 2004**

Mark J. Rozman, Reg. No. 42,117
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024

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PATENT TRADEMARK OFFICE

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Signature of Person Mailing Correspondence

Jennifer Juarez

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	CHRISTOPHER J. KEMP; CHRISTOPH P. MENZEL	§	Group Art Unit:	2836
Serial No.:	09/751,993	§	Examiner:	Roberto Jose Rios Cuevas
Filed:	December 29, 2000	§		
For:	CONVERTING SENSED SIGNALS	§	Atty. Dkt. No.:	ITL.0499US (P10386)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicants respectfully appeal from the final rejection mailed August 27, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 011426/0585.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-30. Claims 1-3, 5-13, and 16-30 are pending. Claims 1-3, 5-13 and 16-18 are allowed. Claims 19, 20 and 23-30 are rejected. Claims

Date of Deposit: January 20, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Jennifer Juarez

21 and 22 are objected to as depending from a rejected base claim. Claims 19, 20 and 23-30 are the subject of this appeal.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Rejection, an Amendment was filed on October 16, 2003 (Reply to Paper No. 6) and a Supplemental Reply to Final Action was filed on November 25, 2003. The amendments in both of these papers have been entered (see Advisory Actions mailed November 13, 2003 and December 8, 2003).

V. SUMMARY OF THE INVENTION

Referring to Figure 1, a stylized block diagram of a restraint system 10 is illustrated in accordance with one embodiment of the present invention. In one embodiment, the restraint system 10 may automatically deploy an airbag in the event of an activation worthy impact event. The restraint system 10 may include a control unit 15, a sensing circuit 20 and a deployment block 25. The sensing block 20 may, in one embodiment, provide a pulse density signal that may be indicative of a sudden acceleration or deceleration, for example.

The restraint system 10 may include a control unit 15, a sensing circuit 20 and a deployment block 25. The sensing block 20 may, in one embodiment, provide a pulse density signal that may be indicative of a sudden acceleration or deceleration, for example.

Referring now to Figure 2, a schematic diagram of one embodiment of the sensing circuit 20 of Figure 1 is illustrated. In one embodiment, the sensing circuit 20 includes an input block 217, a sensing block 220, and a converting block 225. The sensing circuit 20 converts an output signal from the sensing block 220 to a digital signal when pre-selected voltages are applied to the sensing block 220 and other nodes of the sensing circuit 20, in accordance with one embodiment of the present invention.

In one embodiment, two non-overlapping clocks, UN (unity) and INT (integrate), are used to clock the sensing circuit 20, as shown in Figure 3. In one embodiment, during the UN clock cycles, selected nodes of the sensing circuit 20 are set to a predefined level, such as to a V_{CM} voltage level, as shown in Figure 3. In one embodiment, the sensing circuit 20 is clocked starting with the UN clock. Figure 3 illustrates an output signal, OUT, which is the output of the sensing circuit 20. See specification, pp. 3-5.

Referring again to Figure 2, the sensing block 220 includes two capacitors, C_A and C_B, connected at a common node. The upward arrow through capacitor C_A indicates that the C_A capacitance may increase in response to an input, which, in one embodiment, may represent acceleration. The downward arrow through capacitor C_B indicates that the C_B capacitance may decrease in response to an input signal. In one embodiment, the sensing block 220, upon sensing acceleration, provides an output signal to the converting block 225. The sensing block 220, in one embodiment, has an input terminal 222 and two output terminals 224, 226. The input terminal 222, in one embodiment, is a common node to the C_A and C_B capacitors.

The converting block 225, in one embodiment, includes an integrator 228 coupled to a comparator 231, which may be further coupled to a latch 234. A differential operational amplifier (opamp) 237, along with feedback capacitors, C_{FN} and C_{FP}, forms the integrator 228, in the illustrated embodiment. In one embodiment, an applied direct current (DC) voltage, V_{CM}, to the opamp 237 sets a common-mode level of the integrator 228.

The integrator 228, in one embodiment, includes two switches 252, 253. During the INT clock phase or cycle (see Figure 3), the switch 252 is in the "INT" (*i.e.,* up) position, and during the UN phase, the switch 252 is in the "UN" (*i.e.,* down) position, in one embodiment.

Similarly, during the INT phase, the switch 253 is in the "INT" position, and during the UN phase, the switch 253 is in the "UN" position, in one embodiment. See specification, pp. 5-7.

The output terminals 246, 248 of the integrator 228 are coupled to respective input terminals of the comparator 231. The comparator 231, in one embodiment, provides an output signal that is a digital "1" if the voltage difference between the output terminals 246, 248 of the integrator 228 is positive, and a digital "0" if it is negative. The differential output voltage (*i.e.*, the voltage at the output terminal 246 minus the voltage at the output terminal 248) of the integrator 228 is denoted herein as V_{OD}.

The output of the comparator 231 is provided to the latch 234, in one embodiment. The latch 234 transfers a "0" or "1" at its input terminal to its output terminal on each falling edge of the INT clock phase (see Figure 3), in one embodiment. The output signal (OUT) of the latch 234 may be a digital bit stream that is fed back into the switches of the input block 217. In one embodiment, the output of the latch 234 is the output of the sensing circuit 20. The density of 1's in the OUT signal may be an indication of the magnitude of the amplitude of the input signal to the sensing block 220.

The sensing circuit 20, in one embodiment, may be calibrated with calibration voltages, V_{CAL1} and V_{CAL2}. In some instances, it may be difficult to fabricate the sensing block 220 with tight tolerances. As such, the sensing circuit 20 may be calibrated by adjusting the V_{CAL1} and V_{CAL2} voltages during a calibration operation after the sensing circuit 20 is assembled. During calibration, V_{CAL1} and V_{CAL2} voltages may be set to values that bring the sensitivity and offset calibration parameters of the sensing circuit 20 within a desirable specification range. After calibration, the V_{CAL1} and V_{CAL2} voltages may remain fixed for the lifetime of the sensing circuit 20.

In one embodiment, a storage unit 235 of the sensing circuit 20 may store the voltages V_{CAL1} and V_{CAL2} in digital form. The storage unit 235 may be a non-volatile programmable memory, such as electrically erasable programmable read-only memory (EEPROM), fuse-blowing memory, or zener-zapping memory. See specification, pp. 7-9.

Both the input capacitors (C_N and C_P) and the sense element capacitors (C_A and C_B) may deliver charge to (or extract charge from) the feedback capacitors (C_{FN} and C_{FP}) in response to the change in position of the switches 270-274. When some or all of the voltages settle to essentially static values at the end of the INT phase, the value of V_{OD} may have changed to a new value. If this new value is positive, then the OUT signal may be a "1" for the next clock cycle. If the new value is negative, then the OUT signal may be a "0" for the next clock cycle.

Providing the OUT signal to the switches 275-276 causes the output voltage (V_{OD}) of the integrator 228 to change (on the INT phase) in a direction that tends to cause the OUT signal to change states (*e.g.,* from zero to one, or vice-versa), in one embodiment. In other words, if V_{OD} on a given clock cycle is positive, then on the next clock cycle it may be either less positive or negative. And if V_{OD} on a given clock cycle is negative, then on the next clock cycle it may be either less negative or positive.

In one embodiment, the value of (C_A - C_B), which is the response of the sensing block differential capacitance to the input excitation, may affect the size of the charge packets delivered to the integrator 228 on each clock cycle, and ultimately affect the fraction of the OUT signal clock cycles that deliver 1's. This fractional pulse density (FPD) is the value of the output signal of the sensing circuit 20, in one embodiment. The FPD, in one embodiment, is defined as the number of clock periods per second having a high output value, divided by the clock frequency.

In one embodiment, during non-triggering events (*e.g.*, no sudden change in acceleration, pressure, etc.), the output of the sensing circuit 20 may be a series of alternating ones and zeros. In the event of a triggering event (*e.g.*, existence of sudden acceleration), there may be an increase in capacitance of capacitor C_A and a decrease in capacitance of capacitor C_B within the sensing block 220, in one embodiment. This differential capacitance (C_A-C_B), in one embodiment, may cause the sensing circuit 20 to output more ones than zeros for a selected time interval.

Referring now to Figure 4, a graphical illustration of the voltage levels and transitions that may be applied to various nodes of the sensing circuit 20 is shown in one embodiment, for both values of the OUT signal. See specification, pp. 13-14.

VI. ISSUES

A. Are Claims 19 and 20 Patentable Under 35 U.S.C. § 102(b) Over Swartz?

B. Is Claim 23 Patentable Under 35 U.S.C. §103(a) Over Swartz In View of Kemp?

C. Is Claim 24 Patentable Under 35 U.S.C. § 103(a) Over Swartz In View Of Kemp?

D. Are Claims 25-30 Patentable Under 35 U.S.C. §103(a) Over Kemp In View of Swartz?

VII. GROUPING OF THE CLAIMS

For purposes of this appeal, the claims do not stand or fall together. For purposes of this appeal, Applicants have grouped together claims 19 and 20, and claims 25-30, as set forth above.

VIII. ARGUMENT

A. Claims 19 and 20 Are Patentable Under 35 U.S.C. § 102(b) Over Swartz

Claims 19 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,642,555 (Swartz). This rejection is improper. Claim 19 recites an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block and a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

Nowhere does Swartz disclose an input signal to be provided to a common terminal of a first capacitor and a second capacitor of a sensing block. In this regard, in Swartz there is no common terminal of the first capacitor and the second capacitor that is provided an input signal. Instead, capacitors 2 and 5 (shown in FIGS. 1 and 2) of Swartz do not have a common terminal that is provided an input signal, as each capacitor is coupled to a different resistor and a different one shot multi-vibrator. Accordingly, there is no common terminal of a first and second capacitor in Swartz. Thus, claim 19 and claim 20 depending therefrom are patentable and the rejection should be reversed.[1]

B. Claim 23 Is Patentable Under 35 U.S.C. §103(a) Over Swartz In View of Kemp

Claim 23 depends from claim 19 and stands rejected under 35 U.S.C. §103(a) over Swartz in view of U.S. Patent No. 5,528,520 (Kemp). As discussed above with regard to claim 19 (*see* VIII.A), Swartz nowhere teaches or suggests an input signal that is provided to a common terminal of a first and second capacitor. Nor does Kemp, as Kemp discloses two capacitors C_A and C_B connected in series. Kemp, col. 2, lns. 36-37; FIG. 1. The common node

[1] Claims 21 and 22 are indicated as being objected to for being dependent from rejected claim 19, and are thus also patentable. *See* Advisory Action mailed December 8, 2003.

between capacitors C_A and C_B of Kemp does not receive an input signal, instead the common node is used as an output. Id. at lns. 40-41.

Thus neither reference teaches or suggests a common terminal of first and second capacitors that is provided an input signal. Thus claim 23 is patentable over the proposed combination and the rejection should be reversed.

C. Claim 24 Is Patentable Under 35 U.S.C. § 103(a) Over Swartz In View Of Kemp

Claim 24 depends from claim 19 and further recites a storage unit to store one or more voltage values to apply to the sensing circuit of claim 19. Dependent claim 24 stands rejected under 35 U.S.C. § 103(a) over Swartz in view Kemp. This rejection is improper.

The Examiner concedes that Swartz does not disclose storing voltages in a storage unit. Final Office Action, p. 3. Instead, the Examiner relies on Kemp, which the Examiner states "teaches a capacitive sensor comprising a memory for storing calibrating voltages (col. 3, ln. 7)." Id.

This proposed combination lacks any valid motivation to combine the individual references. In Kemp, a memory stores calibrating voltages. However, nowhere can such calibrating voltages be used in Swartz. This is true at least for the reason that nothing in Swartz requires a calibrating voltage. Thus there is no motivation to combine the references. As held by the Federal Circuit, "to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the Applicant." *In re Kotzab,* 55 U.S.P.Q.2d 1313 (Fed. Cir. 2002). Because no such motivation is present here, a *prima facie* case of obviousness has not been made.

Further, the proposed modification would change the principle of operation of Swartz, and thus the proposed combination is improper. MPEP §2143.01.

Also, as discussed above in Section VIII.B, neither Swartz nor Kemp teaches or suggests an input signal provided to a common terminal of a first capacitor and a second capacitor of a sensing block, as recited by claim 19 from which claim 24 depends. Thus the rejection of claim 24 should be reversed.

D. Claims 25-30 Are Patentable Under 35 U.S.C. §103(a) Over Kemp In View of Swartz

Independent claim 25 recites a restraint system including a sensing circuit to apply an input signal to a common input terminal of a sensing block. Claim 25 and claims 26-30 depending therefrom stand rejected under 35 U.S.C. §103(a) over Kemp in view of Swartz. The Examiner concedes that Kemp does not "disclose applying an input signal to a common input terminal of the sensing circuit." Final Office Action, p. 4. The Examiner instead relies on Swartz for such a teaching.

However, there is no basis in either reference to modify Kemp such that a common input terminal of a sensing block exists. *See In re Kotzab,* 55 U.S.P.Q.2d at 1313. In this regard, the sensing block of Kemp is sensor 10 which includes two capacitors C_A and C_B connected in series. Kemp, col. 2, lns. 36-37; FIG. 1. Providing an input to a common input terminal of these capacitors would utterly defeat the purpose of Kemp in which the separate input terminals of capacitors C_A and C_B receive different input signals.

Thus the proposed modification would change the basic principle of Kemp that its capacitors be connected in series such that there is no common input terminal, and that different input values are provided to capacitors C_A and C_B (instead of a single input signal to a common

input terminal). *See* Kemp, col. 4, lns. 37-47. Thus for at least this reason the proposed combination is improper and claims 25-30 are patentable and the rejection should be reversed.

IX. CONCLUSION

Since the rejections of the claims are baseless, they should be reversed.

Respectfully submitted,

Date: 1/20/04

Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
8554 Katy Fwy, Ste 100
Houston, TX 77024-1805
512/418-9944 [Phone]
713/468-8883 [Facsimile]

APPENDIX OF CLAIMS

The claims on appeal are:

19. An apparatus, comprising:

an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block; and

a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

20. The apparatus of claim 19, wherein the converting block is coupled to provide a digital signal based on the sensed signal.

21. The apparatus of claim 19, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

22. The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

23. The apparatus of claim 19, wherein the converting block comprises:

an integrator to receive the sensed signal from the sensing block and to produce an integrated signal;

a comparator to receive the integrated signal and to provide an output signal; and

a latch to receive the output signal and to provide a latched output signal.

24. The apparatus of claim 19, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

25. A restraint system, comprising:

a sensing circuit to:

apply an input signal to a common input terminal of a sensing block;

receive a sensed signal from the sensing block in response to applying the input signal; and

provide an output signal based at least in part on the sensed signal; and

a deployment block to provide an activation signal based at least in part on the output signal from the sensing circuit.

26. The restraint system of claim 25, wherein the deployment block is coupled to provide the activation signal to activate an airbag.

27. The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked via a plurality of non-overlapping clocks.

28. The restraint system of claim 25, wherein the sensing circuit is configured to provide a digital signal.

29. The restraint system of claim 25, wherein the sensing circuit is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

30. The restraint system of claim 25, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	CHRISTOPHER J. KEMP; CHRISTOPH P. MENZEL	§	Group Art Unit:	2836
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APPEAL BRIEF

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II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-30. Claims 1-3, 5-13, and 16-30 are pending. Claims 1-3, 5-13 and 16-18 are allowed. Claims 19, 20 and 23-30 are rejected. Claims

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21 and 22 are objected to as depending from a rejected base claim. Claims 19, 20 and 23-30 are the subject of this appeal.

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V. SUMMARY OF THE INVENTION

Referring to Figure 1, a stylized block diagram of a restraint system 10 is illustrated in accordance with one embodiment of the present invention. In one embodiment, the restraint system 10 may automatically deploy an airbag in the event of an activation worthy impact event. The restraint system 10 may include a control unit 15, a sensing circuit 20 and a deployment block 25. The sensing block 20 may, in one embodiment, provide a pulse density signal that may be indicative of a sudden acceleration or deceleration, for example.

The restraint system 10 may include a control unit 15, a sensing circuit 20 and a deployment block 25. The sensing block 20 may, in one embodiment, provide a pulse density signal that may be indicative of a sudden acceleration or deceleration, for example.

Referring now to Figure 2, a schematic diagram of one embodiment of the sensing circuit 20 of Figure 1 is illustrated. In one embodiment, the sensing circuit 20 includes an input block 217, a sensing block 220, and a converting block 225. The sensing circuit 20 converts an output signal from the sensing block 220 to a digital signal when pre-selected voltages are applied to the sensing block 220 and other nodes of the sensing circuit 20, in accordance with one embodiment of the present invention.

In one embodiment, two non-overlapping clocks, UN (unity) and INT (integrate), are used to clock the sensing circuit 20, as shown in Figure 3. In one embodiment, during the UN clock cycles, selected nodes of the sensing circuit 20 are set to a predefined level, such as to a V_{CM} voltage level, as shown in Figure 3. In one embodiment, the sensing circuit 20 is clocked starting with the UN clock. Figure 3 illustrates an output signal, OUT, which is the output of the sensing circuit 20. See specification, pp. 3-5.

Referring again to Figure 2, the sensing block 220 includes two capacitors, C_A and C_B, connected at a common node. The upward arrow through capacitor C_A indicates that the C_A capacitance may increase in response to an input, which, in one embodiment, may represent acceleration. The downward arrow through capacitor C_B indicates that the C_B capacitance may decrease in response to an input signal. In one embodiment, the sensing block 220, upon sensing acceleration, provides an output signal to the converting block 225. The sensing block 220, in one embodiment, has an input terminal 222 and two output terminals 224, 226. The input terminal 222, in one embodiment, is a common node to the C_A and C_B capacitors.

The converting block 225, in one embodiment, includes an integrator 228 coupled to a comparator 231, which may be further coupled to a latch 234. A differential operational amplifier (opamp) 237, along with feedback capacitors, C_{FN} and C_{FP}, forms the integrator 228, in the illustrated embodiment. In one embodiment, an applied direct current (DC) voltage, V_{CM}, to the opamp 237 sets a common-mode level of the integrator 228.

The integrator 228, in one embodiment, includes two switches 252, 253. During the INT clock phase or cycle (see Figure 3), the switch 252 is in the "INT" (*i.e.,* up) position, and during the UN phase, the switch 252 is in the "UN" (*i.e.,* down) position, in one embodiment.

Similarly, during the INT phase, the switch 253 is in the "INT" position, and during the UN phase, the switch 253 is in the "UN" position, in one embodiment. See specification, pp. 5-7.

The output terminals 246, 248 of the integrator 228 are coupled to respective input terminals of the comparator 231. The comparator 231, in one embodiment, provides an output signal that is a digital "1" if the voltage difference between the output terminals 246, 248 of the integrator 228 is positive, and a digital "0" if it is negative. The differential output voltage (*i.e.*, the voltage at the output terminal 246 minus the voltage at the output terminal 248) of the integrator 228 is denoted herein as V_{OD}.

The output of the comparator 231 is provided to the latch 234, in one embodiment. The latch 234 transfers a "0" or "1" at its input terminal to its output terminal on each falling edge of the INT clock phase (see Figure 3), in one embodiment. The output signal (OUT) of the latch 234 may be a digital bit stream that is fed back into the switches of the input block 217. In one embodiment, the output of the latch 234 is the output of the sensing circuit 20. The density of 1's in the OUT signal may be an indication of the magnitude of the amplitude of the input signal to the sensing block 220.

The sensing circuit 20, in one embodiment, may be calibrated with calibration voltages, V_{CAL1} and V_{CAL2}. In some instances, it may be difficult to fabricate the sensing block 220 with tight tolerances. As such, the sensing circuit 20 may be calibrated by adjusting the V_{CAL1} and V_{CAL2} voltages during a calibration operation after the sensing circuit 20 is assembled. During calibration, V_{CAL1} and V_{CAL2} voltages may be set to values that bring the sensitivity and offset calibration parameters of the sensing circuit 20 within a desirable specification range. After calibration, the V_{CAL1} and V_{CAL2} voltages may remain fixed for the lifetime of the sensing circuit 20.

In one embodiment, a storage unit 235 of the sensing circuit 20 may store the voltages V_{CAL1} and V_{CAL2} in digital form. The storage unit 235 may be a non-volatile programmable memory, such as electrically erasable programmable read-only memory (EEPROM), fuse-blowing memory, or zener-zapping memory. See specification, pp. 7-9.

Both the input capacitors (C_N and C_P) and the sense element capacitors (C_A and C_B) may deliver charge to (or extract charge from) the feedback capacitors (C_{FN} and C_{FP}) in response to the change in position of the switches 270-274. When some or all of the voltages settle to essentially static values at the end of the INT phase, the value of V_{OD} may have changed to a new value. If this new value is positive, then the OUT signal may be a "1" for the next clock cycle. If the new value is negative, then the OUT signal may be a "0" for the next clock cycle.

Providing the OUT signal to the switches 275-276 causes the output voltage (V_{OD}) of the integrator 228 to change (on the INT phase) in a direction that tends to cause the OUT signal to change states (*e.g.,* from zero to one, or vice-versa), in one embodiment. In other words, if V_{OD} on a given clock cycle is positive, then on the next clock cycle it may be either less positive or negative. And if V_{OD} on a given clock cycle is negative, then on the next clock cycle it may be either less negative or positive.

In one embodiment, the value of (C_A - C_B), which is the response of the sensing block differential capacitance to the input excitation, may affect the size of the charge packets delivered to the integrator 228 on each clock cycle, and ultimately affect the fraction of the OUT signal clock cycles that deliver 1's. This fractional pulse density (FPD) is the value of the output signal of the sensing circuit 20, in one embodiment. The FPD, in one embodiment, is defined as the number of clock periods per second having a high output value, divided by the clock frequency.

In one embodiment, during non-triggering events (*e.g.*, no sudden change in acceleration, pressure, etc.), the output of the sensing circuit 20 may be a series of alternating ones and zeros. In the event of a triggering event (*e.g.*, existence of sudden acceleration), there may be an increase in capacitance of capacitor C_A and a decrease in capacitance of capacitor C_B within the sensing block 220, in one embodiment. This differential capacitance (C_A-C_B), in one embodiment, may cause the sensing circuit 20 to output more ones than zeros for a selected time interval.

Referring now to Figure 4, a graphical illustration of the voltage levels and transitions that may be applied to various nodes of the sensing circuit 20 is shown in one embodiment, for both values of the OUT signal. See specification, pp. 13-14.

VI. ISSUES

A. Are Claims 19 and 20 Patentable Under 35 U.S.C. § 102(b) Over Swartz?

B. Is Claim 23 Patentable Under 35 U.S.C. §103(a) Over Swartz In View of Kemp?

C. Is Claim 24 Patentable Under 35 U.S.C. § 103(a) Over Swartz In View Of Kemp?

D. Are Claims 25-30 Patentable Under 35 U.S.C. §103(a) Over Kemp In View of Swartz?

VII. GROUPING OF THE CLAIMS

For purposes of this appeal, the claims do not stand or fall together. For purposes of this appeal, Applicants have grouped together claims 19 and 20, and claims 25-30, as set forth above.

VIII. ARGUMENT

A. Claims 19 and 20 Are Patentable Under 35 U.S.C. § 102(b) Over Swartz

Claims 19 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,642,555 (Swartz). This rejection is improper. Claim 19 recites an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block and a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

Nowhere does Swartz disclose an input signal to be provided to a common terminal of a first capacitor and a second capacitor of a sensing block. In this regard, in Swartz there is no common terminal of the first capacitor and the second capacitor that is provided an input signal. Instead, capacitors 2 and 5 (shown in FIGS. 1 and 2) of Swartz do not have a common terminal that is provided an input signal, as each capacitor is coupled to a different resistor and a different one shot multi-vibrator. Accordingly, there is no common terminal of a first and second capacitor in Swartz. Thus, claim 19 and claim 20 depending therefrom are patentable and the rejection should be reversed.[1]

B. Claim 23 Is Patentable Under 35 U.S.C. §103(a) Over Swartz In View of Kemp

Claim 23 depends from claim 19 and stands rejected under 35 U.S.C. §103(a) over Swartz in view of U.S. Patent No. 5,528,520 (Kemp). As discussed above with regard to claim 19 (*see* VIII.A), Swartz nowhere teaches or suggests an input signal that is provided to a common terminal of a first and second capacitor. Nor does Kemp, as Kemp discloses two capacitors C_A and C_B connected in series. Kemp, col. 2, lns. 36-37; FIG. 1. The common node

[1] Claims 21 and 22 are indicated as being objected to for being dependent from rejected claim 19, and are thus also patentable. *See* Advisory Action mailed December 8, 2003.

between capacitors C_A and C_B of Kemp does not receive an input signal, instead the common node is used as an output. Id. at lns. 40-41.

Thus neither reference teaches or suggests a common terminal of first and second capacitors that is provided an input signal. Thus claim 23 is patentable over the proposed combination and the rejection should be reversed.

C. Claim 24 Is Patentable Under 35 U.S.C. § 103(a) Over Swartz In View Of Kemp

Claim 24 depends from claim 19 and further recites a storage unit to store one or more voltage values to apply to the sensing circuit of claim 19. Dependent claim 24 stands rejected under 35 U.S.C. § 103(a) over Swartz in view Kemp. This rejection is improper.

The Examiner concedes that Swartz does not disclose storing voltages in a storage unit. Final Office Action, p. 3. Instead, the Examiner relies on Kemp, which the Examiner states "teaches a capacitive sensor comprising a memory for storing calibrating voltages (col. 3, ln. 7)." Id.

This proposed combination lacks any valid motivation to combine the individual references. In Kemp, a memory stores calibrating voltages. However, nowhere can such calibrating voltages be used in Swartz. This is true at least for the reason that nothing in Swartz requires a calibrating voltage. Thus there is no motivation to combine the references. As held by the Federal Circuit, "to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the Applicant." *In re Kotzab,* 55 U.S.P.Q.2d 1313 (Fed. Cir. 2002). Because no such motivation is present here, a *prima facie* case of obviousness has not been made.

Further, the proposed modification would change the principle of operation of Swartz, and thus the proposed combination is improper. MPEP §2143.01.

Also, as discussed above in Section VIII.B, neither Swartz nor Kemp teaches or suggests an input signal provided to a common terminal of a first capacitor and a second capacitor of a sensing block, as recited by claim 19 from which claim 24 depends. Thus the rejection of claim 24 should be reversed.

D. Claims 25-30 Are Patentable Under 35 U.S.C. §103(a) Over Kemp In View of Swartz

Independent claim 25 recites a restraint system including a sensing circuit to apply an input signal to a common input terminal of a sensing block. Claim 25 and claims 26-30 depending therefrom stand rejected under 35 U.S.C. §103(a) over Kemp in view of Swartz. The Examiner concedes that Kemp does not "disclose applying an input signal to a common input terminal of the sensing circuit." Final Office Action, p. 4. The Examiner instead relies on Swartz for such a teaching.

However, there is no basis in either reference to modify Kemp such that a common input terminal of a sensing block exists. *See In re Kotzab,* 55 U.S.P.Q.2d at 1313. In this regard, the sensing block of Kemp is sensor 10 which includes two capacitors C_A and C_B connected in series. Kemp, col. 2, lns. 36-37; FIG. 1. Providing an input to a common input terminal of these capacitors would utterly defeat the purpose of Kemp in which the separate input terminals of capacitors C_A and C_B receive different input signals.

Thus the proposed modification would change the basic principle of Kemp that its capacitors be connected in series such that there is no common input terminal, and that different input values are provided to capacitors C_A and C_B (instead of a single input signal to a common

input terminal). *See* Kemp, col. 4, lns. 37-47. Thus for at least this reason the proposed combination is improper and claims 25-30 are patentable and the rejection should be reversed.

IX. CONCLUSION

Since the rejections of the claims are baseless, they should be reversed.

Respectfully submitted,

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Mark J. Rozman
Registration No. 42,117
TROP, PRUNER & HU, P.C.
8554 Katy Fwy, Ste 100
Houston, TX 77024-1805
512/418-9944 [Phone]
713/468-8883 [Facsimile]

APPENDIX OF CLAIMS

The claims on appeal are:

19. An apparatus, comprising:

an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block; and

a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

20. The apparatus of claim 19, wherein the converting block is coupled to provide a digital signal based on the sensed signal.

21. The apparatus of claim 19, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

22. The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

23. The apparatus of claim 19, wherein the converting block comprises:

an integrator to receive the sensed signal from the sensing block and to produce an integrated signal;

a comparator to receive the integrated signal and to provide an output signal; and

a latch to receive the output signal and to provide a latched output signal.

24. The apparatus of claim 19, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

25. A restraint system, comprising:

a sensing circuit to:

apply an input signal to a common input terminal of a sensing block;

receive a sensed signal from the sensing block in response to applying the input signal; and

provide an output signal based at least in part on the sensed signal; and

a deployment block to provide an activation signal based at least in part on the output signal from the sensing circuit.

26. The restraint system of claim 25, wherein the deployment block is coupled to provide the activation signal to activate an airbag.

27. The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked via a plurality of non-overlapping clocks.

28. The restraint system of claim 25, wherein the sensing circuit is configured to provide a digital signal.

29. The restraint system of claim 25, wherein the sensing circuit is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

30. The restraint system of claim 25, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.